#8 6-13-2

Express Mail Label No. EL711265762US
Attorney's Docket No. S1022/8547

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: S1022/8547
Serial No.: Unassigned
Filing Date: Herewith
For: A METHOD OF REDUCING DELAYS

Examiner: Unassigned
Art Unit: Unassigned

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir/Madam:

Prior to examination please amendment the above-identified application as follows.

IN THE ABSTRACT

On page 38, line 3, delete "comprises" and insert --includes--.

On page 38, line 4, delete "analogue" and insert --analog--.

On page 38, line 6, delete "analogue" and insert --analog--.

IN THE CLAIMS

Please amend the claims as follows:

A1

1. (Amended) A method of reducing delays in an [analogue] analog simulation model of a hardware circuit comprising the steps of:

stimulating via an input an output of said [analogue] analog model, said output and said input having a relatively high resistance therebetween; and

applying a pulse to a relatively low resistance, whereby when said pulse is applied to the relatively low resistance, the input is connected to said output via the relatively low resistance so that the time constant of the circuit is reduced.

A2

3. (Amended) A method according to claim 1 [or 2], wherein in said step of applying a pulse, the output is connected to a voltage source having a high drive strength for